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Ing-Jer Huang; Tai-An Lu;
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2 **IGBT model validation for soft-switching applications**
Berning, D.W.; Hefner, A.R., Jr.;
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Page(s): 683 -691 vol.1

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3 **From design-for-test to design-for-debug-and-test: analysis of requirements and limitations for 1149.1**
Alves, G.R.; Ferreira, J.M.M.;
VLSI Test Symposium, 1999. Proceedings. 17th IEEE , 25-29 April 1999
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4 **Engineering change protocols for behavioral synthesis**
Kirovski, D.; Potkonjak, M.;
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5 **Developing with the world's fastest 8-bit microcontroller**
Scanlan, D.;
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6 **Enhanced visibility and performance in functional verification by reconstruction**
Marantz, J.;
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7 **Debugging aids for systems-on-a-chip**
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8 **Debugging aids for systems-on-a-chip**
Bannatyne, R.;
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Page(s): 107 -111

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9 **Design and simulation of a RISC-based 32-bit embedded on-board computer**
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10 **Processor-core based design and test**
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Parker, K.P.; McDermid, J.E.; Browen, R.A.; Nuriya, K.; Hirayama, K.; Matsuzawa, A.;
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14 **Logic emulation with virtual wires**
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15 **Combining Visual TEST with ICE for embedded system testing**
Finkelman, D.;
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16 **Testing and diagnosis of board interconnects in microprocessor-based systems**
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18 **Software development tools for embedded systems**
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19 **Radiation evaluation of the 80C186 16-bit microprocessor utilizing an in-circuit emulator for in-situ electrical biasing and characterization**
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Dahl, M.; Babb, J.; Tessier, R.; Hanono, S.; Hoki, D.; Agarwal, A.;
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[Abstract] [PDF Full-Text (672 KB)] **IEEE CNF**

22 **Using IEEE-1149.1 for in-circuit emulation**
Winters, M.;
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23 **An in-circuit emulator for TMS320C25**
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25 **A three-million-transistor microprocessor**
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31 **Logic cell emulation for ASIC in-circuit emulators**
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Hasslen, R.J.; Zafar, N.;

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Yau, C.W.; Jarwala, N.;
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36 **Test program development using multiple test strategies**
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37 **An expert system for the functional specification of test programs**
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38 **In-circuit-emulation in ASIC architectural core designs**
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2 **Using windows messaging to control automatic test equipment**
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Ratan K. Cuha
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Steven J. E. Wilton
Proceedings of the 1998 ACM/SIGDA sixth international symposium on Field programmable gate arrays March 1998
It has become clear that large embedded configurable memory arrays will be essential in future FPGAs. Embedded arrays provide high-density high-speed implementations of the storage parts of circuits. Unfortunately, they require the FPGA vendor to partition the device into memory and logic resources at manufacture-time. This leads to a waste of chip area for customers that do not use all of the storage provided. This chip area need not be wasted, and can in fact be used very efficien ...

7 A design for testability technique for RTL circuits using control/data flow extraction 77%
Indradeep Ghosh , Anand Raghunathan , Niraj K. Jha
Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design January 1997

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1 Guidelines for creating a debuggable processor 80%
R. E. McLear , D. M. Scheibelhut , E. Tammaru
Proceedings of the first international symposium on Architectural support for programming languages and operating systems March 1982
Hardware without software is of little use. Systems that ease the task of debugging software reduce cost and speed development. This paper presents guidelines for designing processors that ease debugging for real-time computer systems. Special hardware can aid the debugging process by tracing execution and accesses to memory. Such hardware requires access to signals that may not be readily available. Other, less exotic hardware provides an interface to the programmer and other processors. T ...

2 A structural view of the Cedar programming environment 80%
Daniel C. Swinehart , Polle T. Zellweger , Richard J. Beach , Robert B. Hagmann
ACM Transactions on Programming Languages and Systems (TOPLAS) August 1986
Volume 8 Issue 4
This paper presents an overview of the Cedar programming environment, focusing on its overall structure—that is, the major components of Cedar and the way they are organized. Cedar supports the development of programs written in a single programming language, also called Cedar. Its primary purpose is to increase the productivity of programmers whose activities include experimental programming and the development of prototype software systems for a high-performance personal computer. T ...

3 IS '97: model curriculum and guidelines for undergraduate degree programs in information systems 80%
Gordon B. Davis , John T. Gorgone , J. Daniel Couger , David L. Feinstein , Herbert E. Longenecker
ACM SIGMIS Database , Guidelines for undergraduate degree programs on Model curriculum and guidelines for undergraduate degree programs in information systems December 1997
Volume 28 Issue 1

4 A user's viewpoint on the Programmer's Workbench 77%
M. H. Bianchi , J. L. Wood
Proceedings of the 2nd international conference on Software engineering October 1976
The Programmer's Workbench boasts a broad set of highly useful features aimed at the application program developer. It claims to be a "human-end" computer providing tools and services to ease the load on the application system designer, programmer, documenter, tester, and delivery personnel. This paper shows the benefits of using the PWB tools, individually and in combination. Through specific examples drawn from the history of a software project, evidence is given that the use ...

5 Simulating modular microcomputers 77%
Frank J. Langley , Gerald A. LaGro , Joan Sheehan
Proceedings of the eleventh annual simulation symposium March 1978
The commitment of microprocessor-based system configurations to detailed logic design and breadboard fabrication traditionally results in a costly development cycle. This paper reports on the use of a computer design high-order-language (HOL) to simulate micro-computer functional elements, "macromodules", at the register level, and verify the timing and interface requirements for a family of microcomputer configurations. The definitions of these microcomputer macromodules (i. e. ...

6 The automated generation of cross-system software for supporting micro/mini computer systems 77%
Gearold R. Johnson , Robert A. Mueller
Proceedings of the ACM SIGMINI/SIGPLAN interface meeting on Programming systems in the small processor environment March 1976
ASM/GEN and SIM/GEN are a software system comprised of a set of independent FORTRAN program writer modules designed to generate micro computer and small minicomputer assemblers and simulators. It is simple enough to be used by those with limited architecture and programming backgrounds, but flexible and powerful enough to generate efficient and well-structured assemblers and simulators for small micro/mini computers with sophisticated architectures and instruction sets. This paper presents ...

7 Capability requirements in a multimicro processor, hardware/software simulation environment 77%
Paul J. Drongowski
Proceedings of the Symposium on Design Automation and Microprocessors February 1977
As part of the research into computer assisted development of microprocessor based systems, a set of target machine independent software tools have been developed for the PDP-11. This set of tools includes a general microassembler and simulator system. The development software adapts to target processors through the use of machine descriptions in a register transfer notation. This report discusses some of the requirements placed upon a simulator system in a multimicro processor, hardware/so ...

8 Computer-aided digital autopilot design & analysis: Methodology, implementation and verification 77%
W. V. Albanes , J. B. Meadows
Proceedings of the 11th conference on Winter simulation - Volume 1 December 1979
This paper details the design methodology for a missile digital autopilot using a digitization approach, and a discrete domain design approach. These two designs rely heavily on computerized system analysis tools in the frequency and time domains. Further, three complex frequency planes are available to the designer, therefore, relative merits of each will be discussed. This paper will also detail the implementation of the autopilot on the missile microcomputer, a six degree of f ...

9 The micro-architecture of the ECLIPSE® MV/8000: Conception and implementation 77%
Jonathan S. Blau , Charles J. Holland , David L. Keating
Proceedings of the 13th micro-programming workshop on Microprogramming November 1980
The microcode of the ECLIPSE MV/8000 controls the hardware to emulate an instruction set. In the MV/8000 the micro-architecture is defined and limited by the following constraints: 1) the desire to implement microcode in a limited number of locations; 2) the use of LSI technology; 3) a virtual memory architecture. This paper will attempt to show how each of these factors contributed to the micro-architecture, to describe that architecture, and to relat ...

10 Architectural considerations for a microprogrammable emulating engine using bit-slices 77%
C. Halatsis , A. van Dam , J. Joosten , M. Letheren
Proceedings of the 7th annual symposium on Computer Architecture May 1980
This paper describes architectural considerations which led to the design of a fast programmable processor made from ECL bit-slioes. The processor will be used as an on-line data filtering engine for high energy physics experiments. Unlike prior designs of such engines, the processor supports both user (horizontal) microcode and emulation of the PDP-11 fixed point instruction set (without memory management and multiple interrupt levels). In addition to an overview of the techniques used to ...

11 THEMIS logic simulator - a mix mode, multi-level, hierarchical, interactive digital circuit simulator 77%
Mahesh H. Doshi , Roderick B. Sullivan , Donald M. Schuler
21st Proceedings of the Design Automation Conference on Design automation June 1984
A new logic simulator called THEMISTM Logic Simulator for the design of LSI, VLSI and PCBs is described. THEMIS supports design verification and test development from initial specification in behavioral and RTL languages to analysis of the final layout at the gate and switch level. To allow the simulation of an entire system or check the correctness of a single circuit, the different modeling techniques can be easily intermixed. THEMIS is a highly interactive simulator ...

12 Supporting reference and dirty bits in SPUR's virtual address cache 77%
D. A. Wood , R. H. Katz
ACM SIGARCH Computer Architecture News , Proceedings of the 16th annual international symposium on Computer architecture April 1989
Volume 17 Issue 3
Virtual address caches can provide faster access times than physical address caches, because translation is only required on cache misses. However, because we don't check the translation information on each cache access, maintaining reference and dirty bits is more difficult. In this paper we examine the trade-offs in supporting reference and dirty bits in a virtual address cache. We use measurements from a uniprocessor SPUR prototype to evaluate different alternatives. The prototype's buil ...

13 Distributed operating systems 77%
Andrew S. Tanenbaum , Robbert Van Renesse
ACM Computing Surveys (CSUR) December 1985
Volume 17 Issue 4
Distributed operating systems have many aspects in common with centralized ones, but they also differ in certain ways. This paper is intended as an introduction to distributed operating systems, and especially to current university research about them. After a discussion of what constitutes a distributed operating system and how it is distinguished from a computer network, various key design issues are discussed. Then several examples of current research projects are examined in some detail ...

14 Statemate: a working environment for the development of complex reactive systems 77%

D. Harel , H. Lachover , A. Naamad , A. Pnueli , M. Politi , R. Sherman , a. Shtul-Trauring

Proceedings of the 10th international conference on Software engineering April 1988

This paper provides a brief overview of the STATEMATE system, constructed over the past three years by i-Logix Inc., and Ad Cad Ltd. STATEMATE is a graphical working environment, intended for the specification, analysis, design and documentation of large and complex reactive systems, such as real-time embedded systems, control and communication systems, and interactive software. It enables a user to prepare, analyze and debug diagrammatic, yet precise, descriptions of the system under devel ...

15 Monitoring and performance measuring distributed systems during operation 77%

D. Wybranietz , D. Haban

Proceedings of the 1988 ACM SIGMETRICS conference on Measurement and modeling of computer systems May 1988

This paper describes an integrated tool for monitoring distributed systems continuously during operation. A hybrid monitoring approach is used. As special hardware support a test and measurement processor (TMP) was designed, which is part of each node in an experimental multicomputer system. Each TMP runs local parts of the monitoring software for its node, while all the TMPs are connected to a central test station via a separate TMP interconnection network. The monitoring system is transpa ...

16 The fuzzball 77%

D. L. Mills

ACM SIGCOMM Computer Communication Review , Symposium proceedings on Communications architectures and protocols August 1988

Volume 18 Issue 4

The Fuzzball is an operating system and applications library designed for the PDP11 family of computers. It was intended as a development platform and research pipewrench for the DARPA/NSF Internet, but has occasionally escaped to earn revenue in commercial service. It was designed, implemented and evolved over a seventeen-year era spanning the development of the ARPANET and TCP/IP protocol suites and can today be found at Internet outposts from Hawaii to Italy standing watch for adventurou ...

17 Structured Programming with go to Statements 77%

Donald E. Knuth

ACM Computing Surveys (CSUR) December 1974

Volume 6 Issue 4

18 The evolution of the Sperry Univac 1100 series: a history, analysis, and projection 77%

B. R. Borgerson , M. L. Hanson , P. A. Hartley

Communications of the ACM January 1978

Volume 21 Issue 1

The 1100 series systems are Sperry Univac's large-scale mainframe computer systems. Beginning with the 1107 in 1962, the 1100 series has progressed through a succession of eight compatible computer models to the latest system, the 1100/80, introduced in 1977. The 1100 series hardware architecture Is based on a 36-bit word, ones complement structure which obtains one operand from storage and one from a high-speed register, or two operands from high-speed registers. The 1100 Operating System ...

19 On the emulation of flowcharts by decision tables 77%

Art Lew

Communications of the ACM December 1982

Volume 25 Issue 12

Any flowchart can be emulated by a decision table, whose complexity depends on that of the flowchart. It may be necessary, however, to introduce a new control variable with associated tests and sets or to permit changes in execution sequences provided action-test independence holds. Two measures of decision table complexity are discussed and interrelated. Finally, conditions and procedures for reducing complexity are presented.

20 Development and application of NASA's first standard spacecraft computer 77%

Charles E. Trevathan , Thomas D. Taylor , Raymond G. Hartenstein , Ann C. Merwarth , William N. Stewart

Communications of the ACM September 1984

Volume 27 Issue 9

To provide the autonomy needed by low, earth-orbiting satellites, NASA's first standard on-board processor requires changing only interfacing hardware from mission to mission.

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21 Creat 77%
Nick Bailey
Linux Journal January 1999
An Embedded Systems Project: CREAT is a tool set for teaching embedded systems. In designing it, Mr. Bailey wanted it to be useful for real problems, cheap enough to build on the pittance which is an undergraduate's project budget, and totally open<

22 Advances in functional abstraction from structure 77%
Richard H. Lathrop , Robert J. Hall , Gavan Duffy , K. Mark Alexander , Robert S. Kirk
Proceedings of the 25th ACM/IEEE conference on Design automation June 1988
FUNSTRUX has been extended to extract behavioral level models for a commercial simulator directly from a circuit netlist. Recent advances include: a retargetable code generation mechanism; an object-oriented control structure; handling of initialization values; and improved run-time and space requirements of the abstraction process. We discuss some of the issues that arise in translating from LISP to 'C' and from one functional paradigm to another.

23 Constructing instruction traces from cache-filtered address traces (CITCAT) 77%
Charlton D. Rose , J. Kelly Flanagan
ACM SIGARCH Computer Architecture News December 1996
Volume 24 Issue 5
Instruction traces are useful tools for studying many aspects of computer systems, but they are difficult to gather without perturbing the systems being traced. In the past, researchers have collected instruction traces through various techniques, including single-stepping, instruction inlining, hardware monitoring, and processor simulation. These approaches, however, fail to produce accurate traces because they interfere with the processor's normal execution.Because processors are deterministic ...

24 Automatic performance prediction to support cross development of parallel programs 77%
Matthias Schumann
Proceedings of the SIGMETRICS symposium on Parallel and distributed tools January 1996

25 The performance impact of flexibility in the Stanford FLASH multiprocessor 77%
Mark Heinrich , Jeffrey Kuskin , David Ofelt , John Heinlein , Joel Baxter , Jaswinder Pal Singh , Richard Simoni , Kourosh Gharachorloo , David Nakahira , Mark Horowitz , Anoop Gupta , Mendel Rosenblum , John Hennessy
Proceedings of the sixth international conference on Architectural support for programming languages and operating systems November 1994
Volume 29 , 28 Issue 11 , 5
A flexible communication mechanism is a desirable feature in multiprocessors because it allows support for multiple communication protocols, expands performance monitoring capabilities, and leads to a simpler design and debug process. In the Stanford FLASH multiprocessor, flexibility is obtained by requiring all transactions in a node to pass through a programmable node controller, called MAGIC. In this paper, we evaluate the performance costs of flexibility by comparing the performance of ...

26 Hardware acceleration of logic simulation using a data flow microarchitecture 77%

G. Catlin , B. Paseman

ACM SIGMICRO Newsletter , Proceedings of the 18th annual workshop on Microprogramming December 1985

Volume 16 Issue 4

Current digital logic simulators running on engineering workstations lack capacity and speed. This paper discusses a hardware accelerator for a workstation simulator which addresses these problems. The accelerator runs 100x faster than its software counterpart and can simulate up to 1 million gates. The accelerator has been built and is being sold commercially. The architecture of the accelerator is similar to that of a classical dataflow machine. We describe the architecture of the machine ...

27 Launching the new era 77%

Kazuhiro Fuchi , Robert Kowalski , Koichi Furukawa , Kazunori Ueda , Ken Kahn , Takashi Chikayama , Evan Tick

Communications of the ACM March 1993

Volume 36 Issue 3

28 Efficient data breakpoints 77%

Robert Wahbe

ACM SIGPLAN Notices , Proceedings of the fifth international conference on Architectural support for programming languages and operating systems September 1992

Volume 27 Issue 9

29 Personal distributed computing: the Alto and Ethernet hardware 77%

Chuck Thacker

Proceedings of the ACM Conference on The history of personal workstations January 1986

Between 1972 and 1980, the first distributed personal computing system was built at the Xerox Palo Alto Research Center. The system was composed of a number of Alto workstations connected by an Ethernet local network. It also included servers that provided centralized facilities. This paper describes the development of the hardware that was the basis of the system.

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